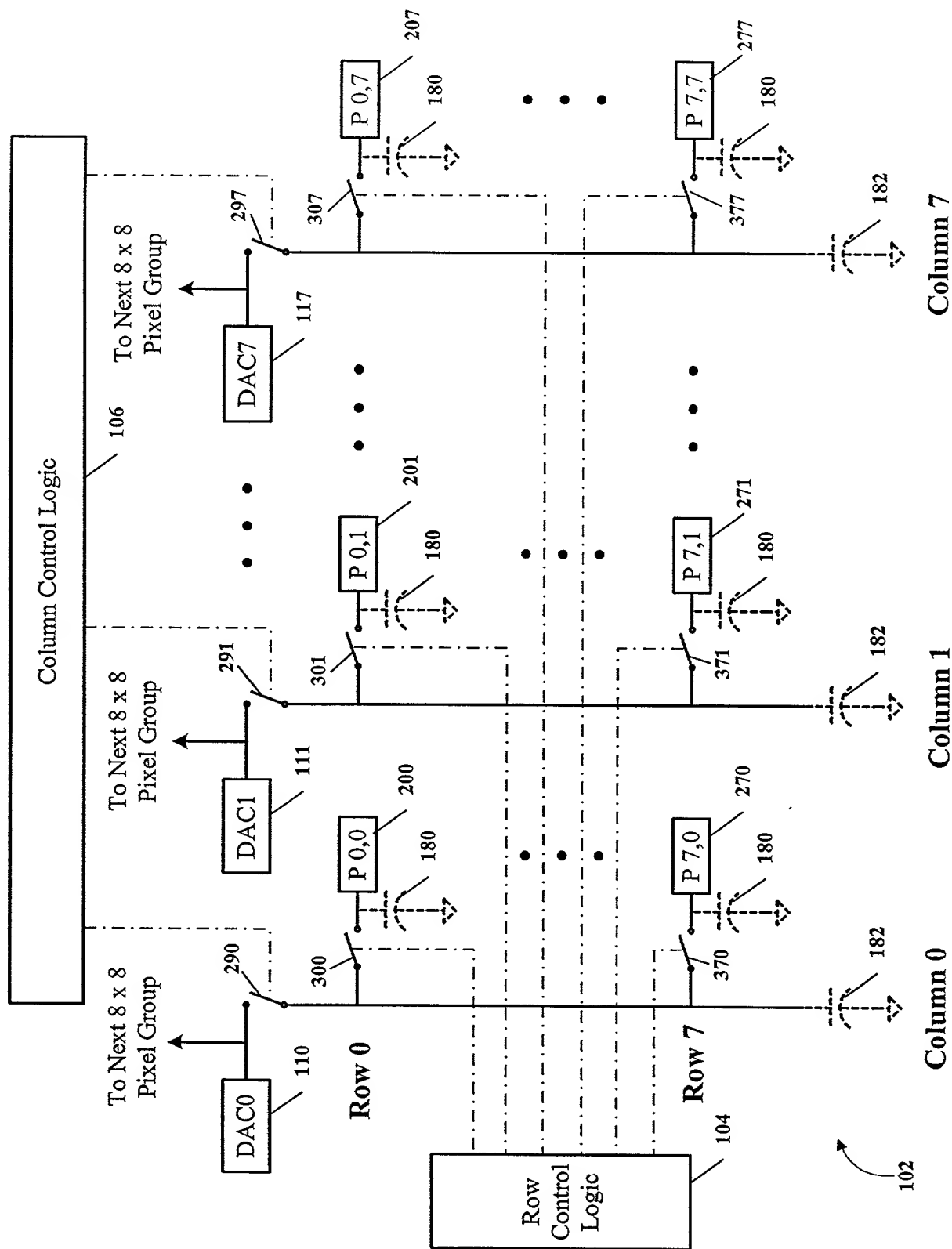




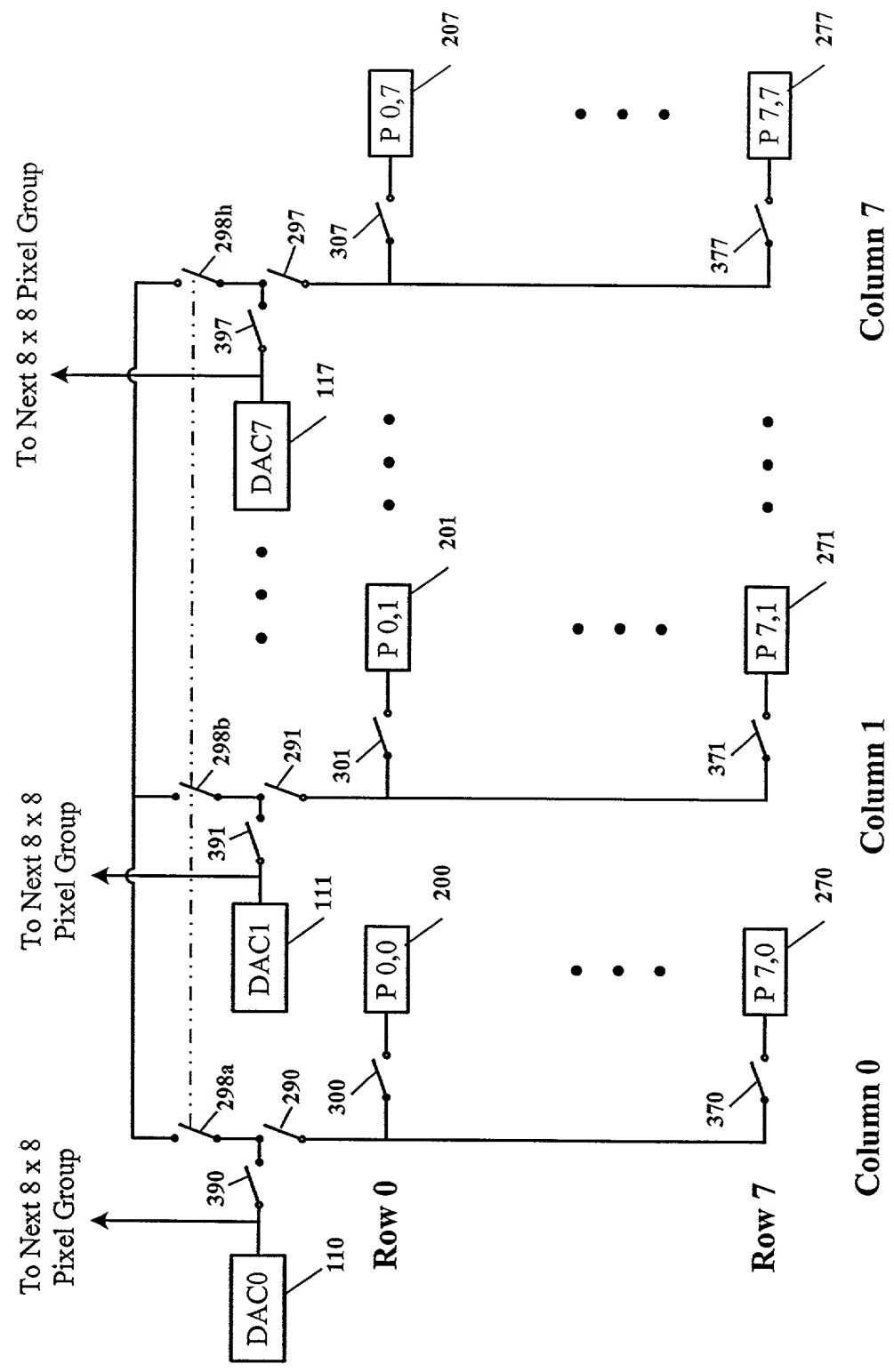
# FIGURE 1

FIG. 2 is a schematic diagram of a pixel array 102, showing a grid of pixel elements (180) arranged in rows (Row 0 to Row 7) and columns (Column 0 to Column 7). The array is controlled by Row Control Logic (104) and Column Control Logic (106). Each pixel element (180) is connected to a row line (300-377) and a column line (290-297). The row lines are controlled by Row Control Logic (104) and the column lines are controlled by Column Control Logic (106). The column lines are also connected to DACs (110-117) and are labeled "To Next 8 x 8 Pixel Group".

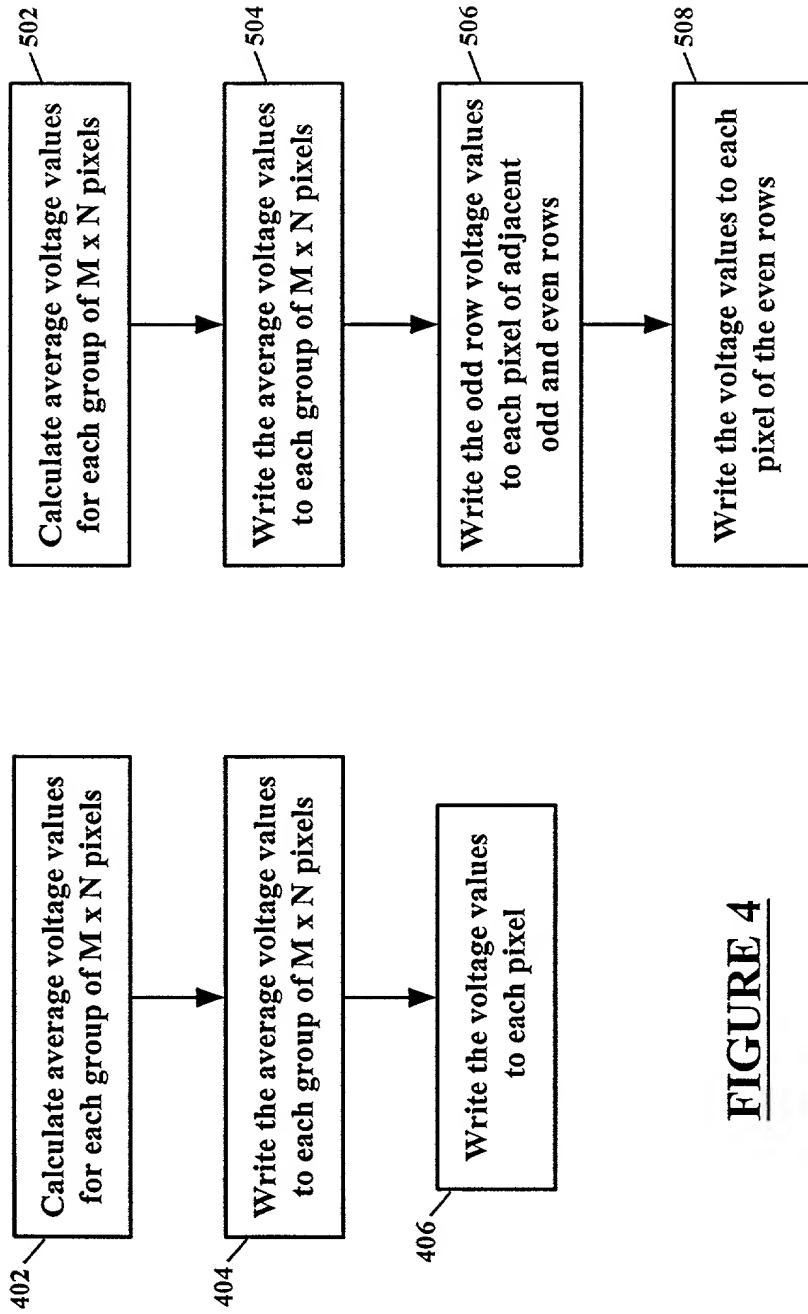


**FIGURE 2**

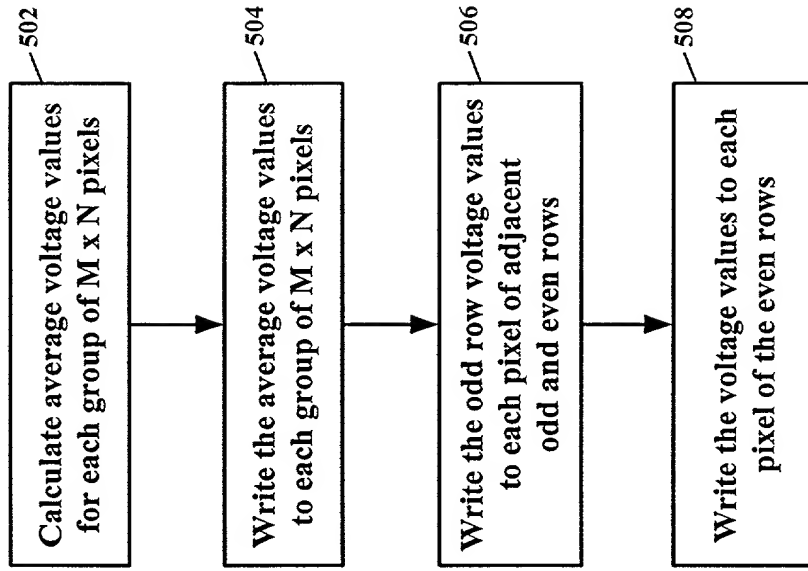
FIG. 3 is a schematic diagram of a pixel array circuit. The circuit includes a row of DACs (110, 111, 117) and a column of DACs (200, 201, 207). The DACs are connected to a grid of switches (300, 301, 307) and output nodes (270, 271, 277). The circuit is divided into three sections: 'To Next 8 x 8 Pixel Group', 'To Next 8 x 8 Pixel Group', and 'To Next 8 x 8 Pixel Group'.



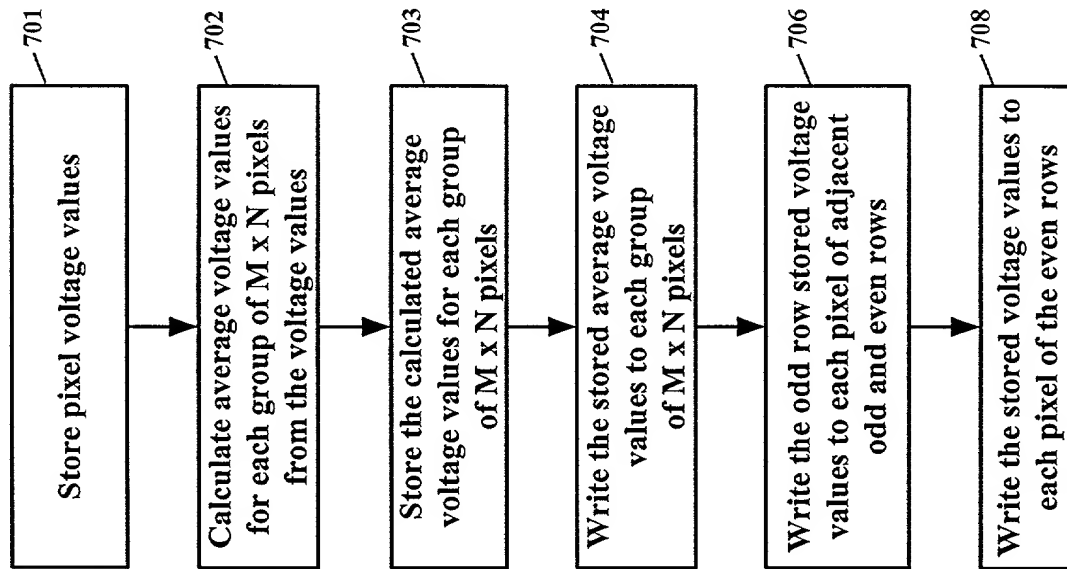
**FIGURE 3**



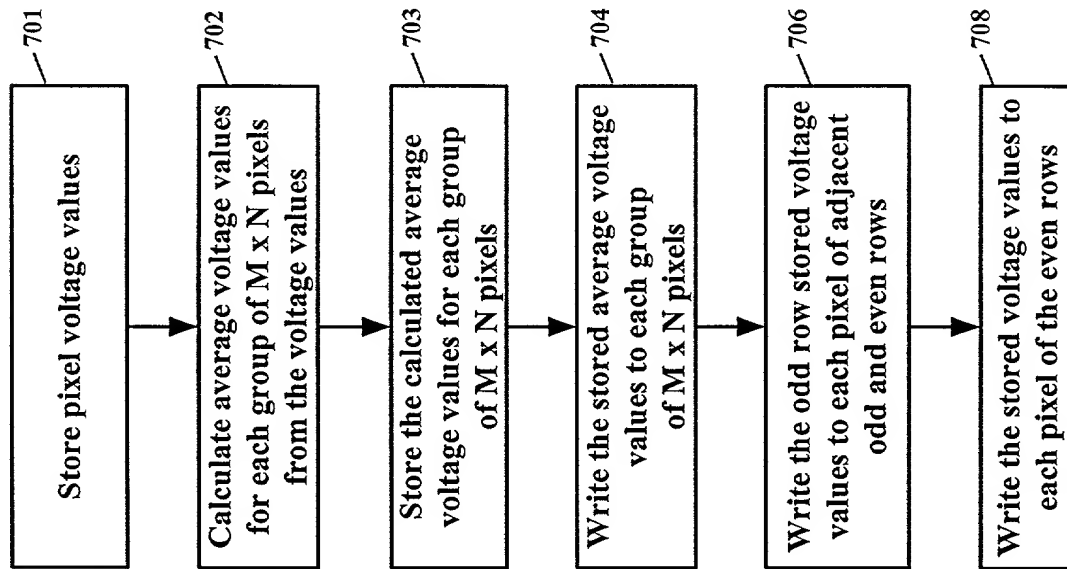
**FIGURE 4**



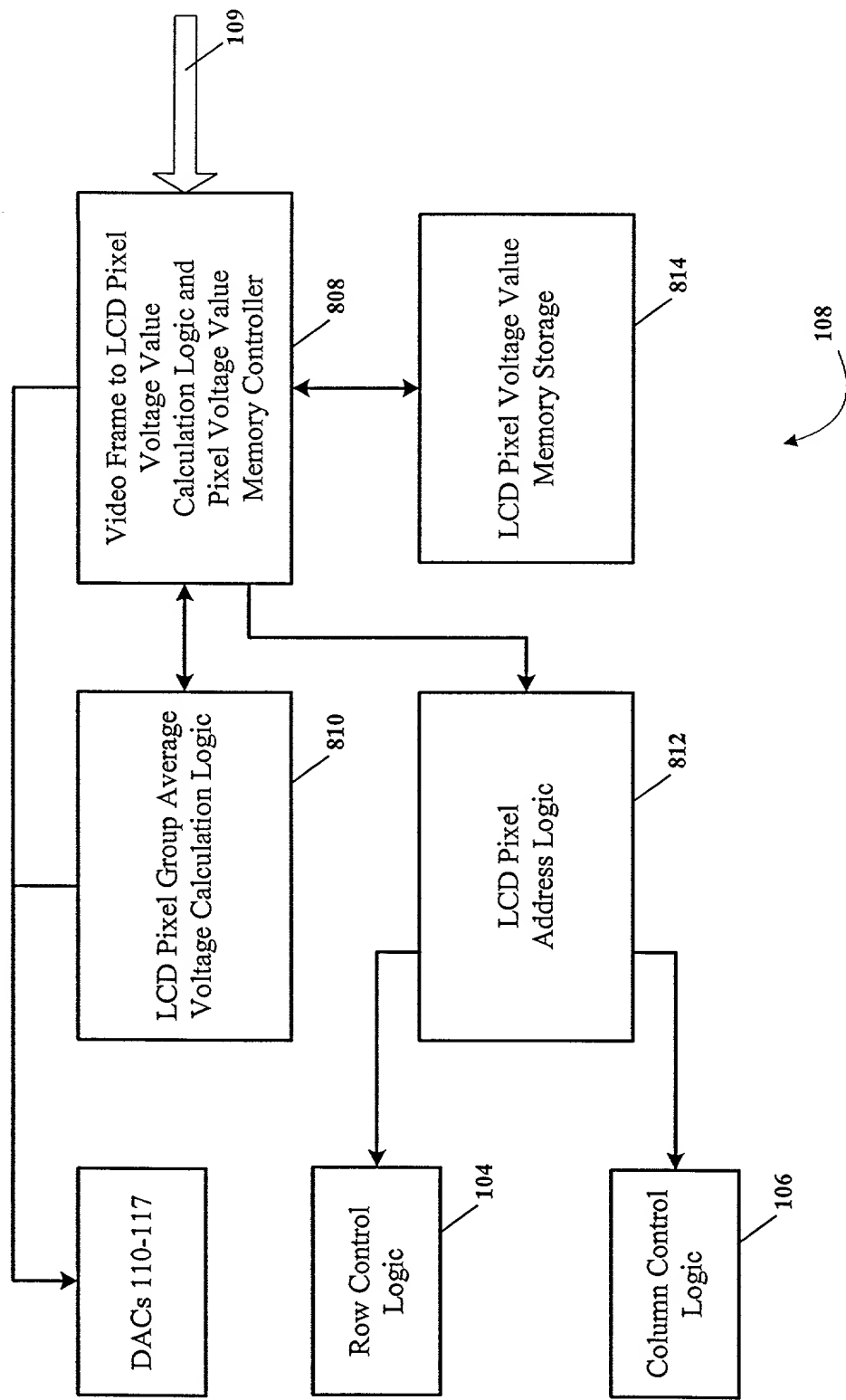
**FIGURE 5**



**FIGURE 6**



**FIGURE 7**



**FIGURE 8**